wider than lower portions **255**, as depicted in FIG. **2**K. In one embodiment, upper portion **265** is at least 10 Angstroms wider than lower portion **255**. In another embodiment, the width of upper portion **265** at the top surface of lower portion **255** is in the range of 40-400 Angstroms. In an embodiment, upper portion **265** directly overlaps source/drain region **218**, as depicted in FIG. **2**K. In one embodiment, upper portion **265** directly overlaps source/drain region **218** by at least 10 Angstroms. In an embodiment, a wet chemical cleaning process step comprising the application of an aqueous solution of hydrofluoric acid, ammonium fluoride or both follows the formation of upper portions **265**.

[0033] Thus, referring to FIG. **2**K, a planar MOS-FET **200** comprising a multi-component low-k isolation spacer may be formed via a replacement isolation spacer process. Planar MOS-FET **200** may be an N-type or a P-type semiconductor device and may be incorporated into an integrated circuit by conventional process steps, as known in the art. As will be appreciated in the typical integrated circuit, both N- and P-channel transistors may be fabricated in a single substrate or epitaxial layer to form a CMOS integrated circuit.

[0034] As depicted in FIGS. **2**A-K, epitaxial source/drain region **218** may have a facet-less sidewall and may thus be flush with sacrificial isolation spacer **235**. In accordance with an embodiment of the present invention, lower portion **255** has a top surface width substantially equal to the width of sacrificial isolation spacer **235**. In one embodiment, the top surface width of lower portion **255** is in the range of 30-250 Angstroms. Alternatively, the epitaxial source/drain region may comprise a faceted sidewall. Referring to FIG. **3**, epitaxial source/drain region **318** has a faceted sidewall **380**. In accordance with an embodiment of the present invention, lower portion **355** has a width greater than the width of the sacrificial isolation spacer. In one embodiment, the top surface width of lower portion **355** is in the range of 75-250 Angstroms. In an embodiment, upper portion **365** directly overlaps source/drain region **318**, as depicted in FIG. **3**. In one embodiment, upper portion **365** directly overlaps source/drain region **318** by at least 10 Angstroms.

[0035] The present invention is not limited to the formation of planar MOS-FETs comprising multi-component low-k isolation spacers. For example, in accordance with an embodiment of the present invention, a bipolar transistor, a memory transistor or a micro-electronic machine (MEM) comprising multi-component low-k isolation spacers is formed. Also, in accordance with another embodiment of the present invention, devices with a three-dimensional architecture, such as independently accessed double gate devices, FIN-FETs, tri-gate devices and gate-all-around devices, are formed incorporating multi-component low-k isolation spacers.

[0036] Therefore, a multi-component low-k isolation spacer and its method of formation for use with a conductive region in a semiconductor structure has been described. In one embodiment, a replacement isolation spacer process is utilized to enable the formation of a two-component low-k isolation spacer directly adjacent to the sidewall of a conductive region in a semiconductor device.

What is claimed is:

1. A semiconductor structure comprising:

a substrate;

a conductive region, wherein said conductive region is above said substrate; and

a multi-component dielectric spacer comprised of a first portion and a second portion, wherein the height of said first portion is less than the height of a sidewall of said conductive region, wherein said first portion is above said substrate and directly adjacent to said sidewall of said conductive region, wherein said second portion is directly above said first portion and is directly adjacent to said sidewall of said conductive region, and wherein the dielectric constant of said first portion is lower than the dielectric constant of said second portion.

2. The structure of claim **1** wherein the dielectric constant of said second portion is at least twice the dielectric constant of said first portion.

3. The structure of claim **1** wherein the dielectric constant of said first portion is in the range of 2.0-4.0, and wherein the dielectric constant of said second portion is in the range of 4.0-7.5.

4. The structure of claim **3** wherein said first portion is comprised of a material selected from the group consisting of silicon dioxide, a porous film and a fluorinated oxide, and wherein said second portion is comprised of a material selected from the group consisting of silicon nitride, silicon oxy-nitride and carbon-doped silicon nitride.

5. The structure of claim **1** wherein the width of said second portion is greater than the width of said first portion.

6. The structure of claim **5** wherein the width of the top surface of said first portion is in the range of 30-250 Angstroms.

7. A semiconductor device comprising:

a substrate;

a gate dielectric layer, wherein said gate dielectric layer is above said substrate;

a gate electrode, wherein said gate electrode is above said gate dielectric layer;

a source/drain region, wherein the top surface of said source/drain region is above the top surface of said substrate, and wherein a sidewall of said source/drain region is spaced apart from a sidewall of said gate electrode; and

a multi-component dielectric spacer comprised of a first portion and a second portion, wherein the height of said first portion is less than the height of said sidewall of said gate electrode, wherein said first portion is above said substrate and directly between said sidewall of said gate electrode and said sidewall of said source/drain region, wherein said second portion is directly above said first portion and is directly adjacent to said sidewall of said gate electrode, and wherein the dielectric constant of said first portion is lower than the dielectric constant of said second portion.

8. The structure of claim **7** wherein the dielectric constant of said second portion is at least twice the dielectric constant of said first portion.

9. The structure of claim **7** wherein the dielectric constant of said first portion is in the range of 2.0-4.0, and wherein the dielectric constant of said second portion is in the range of 4.0-7.5.

10. The structure of claim **9** wherein said first portion is comprised of a material selected from the group consisting of silicon dioxide, a porous film and a fluorinated oxide, and wherein said second portion is comprised of a material selected from the group consisting of silicon nitride, silicon oxy-nitride and carbon-doped silicon nitride.